Impact of Multiple Write Cycles on the Radiation Sensitivity of NAND Flash Memory Devices

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***Abstract*—The work presented here investigates the impact of multiple write cycles on NAND Flash memory radiation sensitivity. Cobalt 60 tests have been performed in order to study the memory array data corruption evolution with respect to the TID level. Heavy ion tests have also been performed to assess the impact of multiple write cycles on the SEU cross section. The irradiated devices were initialized before irradiation with different numbers of write cycles in separated sectors of the memory array. This configuration allowed studying the number of write cycle influence on the radiation sensitivity.**

***Index Terms*—Data corruption, NAND Flash memory, SEU sensitivity, TID testing.**

I. Introduction

Flash memory devices are of great interest in electronic applications, due to their ability to store large sets of data with non-volatility. They provide a good way to design equipments with interesting storage ability at reasonable cost. However, their sensitivity to Total Ionizing Dose (TID) and Single Event Upset (SEU) is a constraint for their use in space applications, where mass storage capability is a growing need.

Existing studies on the radiation susceptibility of Flash memories tend to study separately the sensitivities to single event upset and total ionizing dose. The response of Floating Gate (FG) cells to heavy ions has already been investigated with respect to the ion LET, energy, incidence angle, etc. [1]. The literature also provides analysis of TID effects on Flash memories through X-ray, γ-ray, proton and electron exposures. The combination of several types of ionizing radiation effects in FG cells has been studied in [2]. This work investigates high-energy proton effects, total dose by proton direct ionization and SEE generated by secondary recoils. More recently, reference [3] shows that the single bit upset cross section in FG cells may increase if the tested sample has been previously exposed to TID, even at levels as low as 50 krad(Si), without any program and erase operations in between. This effect is more significant at low LET values. In particular, the number of FG cell error increases with the TID level with an approximately linear trend. The author attributed this behavior to the combination of the drifts induced by TID and heavy ions.

In order to deal with radiation issues when NAND Flash memories are required, the data corruption induced by TID [4] as well as the SEU sensitivity [5] can be improved by charge accumulation at the floating gate level. It has been demonstrated that charge accumulation can be achieved in NAND flash memory cells by applying multiple write cycles [4]. The work presented here is based on TID and heavy ion test experimental data for which the approach developed in [4][5] has been applied. The aim of this study is to determine the best case for which hardening effects can be obtained when multiplying pre-irradiation write cycles on the device. The practical problems that should be considered before using this approach as hardening method will be discussed. This study was performed with the financial and technical support of the Centre National d'Etudes Spatiales (CNES).

II. Test Procedure

The experiments have been conducted on commercial Flash NAND memory devices from two manufacturers. The selected part references are given in Table I.

TABLE I
PART REFERENCE DESCRIPTION

Manufacturer	Micron	Samsung
Reference	MT29F128G08AJAAAWP	K9WBG08U1M-PCB0
Technology	SLC NAND Flash	SLC NAND Flash
Package	TSOP48	TSOP48
Size	128 Gb	32 Gb
Die number	4	2

A. Pre-irradiation sample initialization

For both references, each part has been split into 7 sectors spread in the memory array. All sectors have been initialized

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before irradiation with a different number of write cycles, ranging from 1 to the maximum specified by manufacturer, in some cases.

All sectors have been written with a checkerboard pattern (e.g. an alternated sequence of ones and zeros). With this pattern, spontaneous read errors have been observed on all tested parts above 1 000 preliminary write cycles, before irradiation. These errors are attributed to write disturbs. As explained in [4], they come from FG cells that should be erased, or "unprogrammed", and normally read as '1', but in fact read as '0' due to the presence of parasitic charges. These charges come from the neighboring cells that have been submitted to charge accumulation. Such cells are referred as disturbed cells in the rest of this document.

It's important to notice that if a single "erase block" command is performed, the charges are completely removed from the FG cells in that block, thus eliminating the effects of charge accumulation, as it has been shown in [4]. In the same way, any further "write" command would add some charges in the FG cells. For these reasons, once the initialization completed, no further write or erase operation has been performed during the whole test campaign in order to keep the initial level of charge accumulation, and therefore the number of write disturbs in each sector, related to the number of write cycles.

For heavy ion testing, the parts have been delidded and tested before initialization. For both reference tested in this study, the large capacity is obtained by stacking several dies, so the top-most die had to be identified before initialization.

B. Test hardware

A specific test-bench has been developed by TRAD. The hardware is based on an FPGA board that can perform read, write and erase operations on the devices. A dedicated algorithm has been designed for the FPGA to perform comparisons between the expected data and the data read from the Device Under Test (DUT). For a given address, if the read data differs from the expected data, a frame containing the address, the expected data and the corrupted data is stored. In order to get the real proportion of corrupted data inside the NAND flash memory, no Error Correction Code (ECC) has been implemented and raw data only have been considered.

The FPGA is driven by a software able to store all erroneous data detected during read operations in separate files. It also ensures the bad block management, because if the bad block list was stored inside the NAND flash memory, it could be impacted by the irradiation. In order to obtain the data corruption rate, at the end of a read operation, the number of erroneous data is compared to the sector size. The same test bench has been used for both TID and heavy ion tests.

In addition, during TID test only, an Automated Test Equipment (ATE) has been used to perform parametric measurements and functionality check at each dose levels. For each part, the block 0 was reserved for the functionality check that consists in the following sequence: erase; verify erase; program; verify.

III. TID TESTING

A. TID test setup

TID irradiations were performed under Co-60 in GAMRAY (TRAD – Toulouse, France). The dose rate was fixed at 650 rad(Si)/h for the Samsung memory and at 210 rad(Si)/h for the Micron.

A preliminary TID test has been performed on 6 parts for both references without applying multiple write cycles. The goal of this test was to determine the maximum dose level acceptable by each reference before showing functional failures, based on parametric and functional testing only.

The Samsung memories have shown a good tolerance to TID, with the first functional failure observed above 300 krad, whereas most of the Micron parts have shown functional failures at 48 krad. All the Micron parts were no longer functional at 53 krad.

Once the total dose limit known for each reference thanks to the preliminary test, the TID campaign has been performed. The first step was the sample initialization, performed according to Table II.

TABLE II
WRITE CYCLE SECTORS FOR THE TID TEST

Part type	Sector number	Sector size (block [a])	Number of write cycles
Samsung	1	100	1
	2	100	10
	3	100	100
	4	50	1 000
	5	10	5 000
	6	10	10 000
	7	10	100 000 [b]
Micron	1	100	1
	2	100	10
	3	100	100
	4	10	1 000
	5	10	10 000
	6	4	60 000 [b]

[a] Block size is 262 144 bytes for the Samsung parts, and 1 048 576 bytes for the Micron parts.
[b] Program/erase cycles endurance specified by the manufacturer

The number of write cycles applied per sector during the initialization phase is given in Table II. Fewer blocs have been tested for large numbers of write cycles in order to limit the initialization duration.

For each reference, 5 parts were biased ON in stand-by mode, 5 parts were biased OFF, and 1 part was kept as a reference and therefore not irradiated – but also initialized.

The TID steps have been adapted to each reference tolerance. The Samsung parts have been measured at: 0, 26, 41, 58, 100, 114, 128, 142, 159, 201, 232, 260 and 356 krad. The Micron parts have been measured at: 0, 15, 20, 24, 29, 33, 48 and 53 krad.

The parametric measurements performed at each dose level were used to check the part functionality. In addition, the data corruption was evaluated at each dose step. The data corruption is defined by the percentage of corrupted address in a sector containing at least one bit in error.

B. TID test results

Two distinct behaviors have been observed on the tested references, due to their different TID tolerance. At the maximum TID level, the electrical parameters are still measurable for the Samsung memory, but the data corruption is close to 100%. The Micron parts have shown functional failures at 48 krad, even if a large proportion of the initial data were not corrupted yet.

For both references, no significant differences in the measurement of the data corruption have been observed between the parts biased ON – in stand-by mode – and OFF. The averaged data corruption values presented on Fig. 1 and Fig. 2 have therefore been calculated over the 10 devices.

Samsung TID test results

Fig. 1 presents the data corruption evolution as a function of the TID level for the Samsung memories. Mean values over the 10 tested parts are given for each sector.

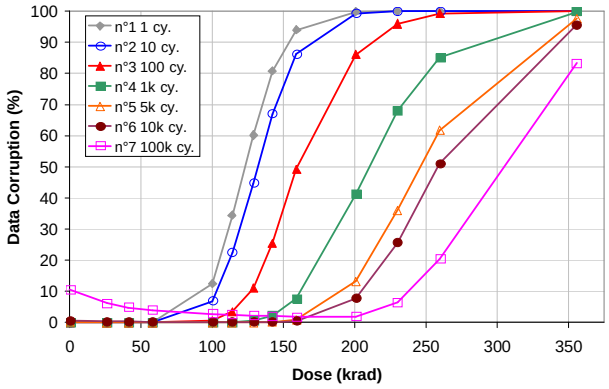

Fig. 1. Data corruption versus TID level – Samsung memory

At 200 krad, all data in the sector n°1 are corrupted. This sector is representative of a typical application where only one write cycle is applied to store data. For sectors submitted to charge accumulation thanks to multiple write cycles, a higher dose level is required to corrupt their content.

The sector n°7, initialized with 100 000 write cycles, shows an initial value of its data corruption around 10% before irradiation. This can be explained by the fact that the preliminary initialization is done by applying an out-of-specification stress to the device, when reaching the datasheet endurance by applying successive write cycles without erase operation. The data corruption in sector n°7 decreases until 200 krad, without any additional write cycle performed. Above 200 krad, the effect of the charge leakage induced by TID irradiation becomes predominant and the content of the sector is progressively erased. At 356 krad, all the FG cells tend to lose their charges.

This observation has been attributed to recovery effects and only concerns the disturbed cells. The recovery effect is only observed for irradiated part, the reference parts (not irradiated) kept their disturbed cell percentage for the whole test duration. This phenomenon has also been reported in [4]. In order to understand the recovery effect induced by radiation, it is reminded that disturbed cells contain charges received from their neighboring FG cells when an intense charge accumulation is achieved. TID irradiation allows these parasitic charges to leak. When the amount of charges in a disturbed cell is low enough to be read again like a '1', the expected data is recovered.

Even if it is not put in evidence on Fig. 1 due to the scale used, the same effect is less significant but also observed for sectors n°4, n°5 and n°6 (respectively initialized with 1 000, 5 000 and 10 000 write cycles). This means that the recovery effect is present each time that disturbed cells are generated.

The Samsung TID test results show that there is a trade-off between the positive diminution of data corruption and the generation of disturbed cells, caused by the application of a large number of write cycles.

Micron TID test results

Fig. 2. presents the data corruption evolution as a function of the TID level for the Micron parts. Mean values over the 10 tested parts are given for each sector.

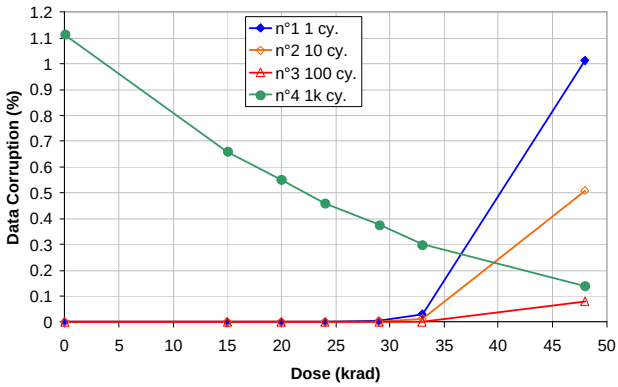

Fig. 2. Data Corruption versus total dose – Micron memory

When write cycles range from 10 to 1 000, an improvement of the radiation tolerance is observed as the number of write cycles increases.

Data corruption for the sectors n°5 and n°6 (resp. initialized with 10 000 and 60 000 write cycles) are not represented on Fig. 2 because almost 100% of their addresses was corrupted after initialization and over the whole test duration. Nevertheless, a small recovery effect for the sector n°5 has been observed – the data corruption evolved from 99.98% after initalization to 99.86% at the maximum dose level. The sector n°6 (maximum endurance specified by the manufacturer) was fully corrupted by disturbed cells after initialization and the recovery effect has not been observed during the test. Almost all the data were stuck at '0' from 0 krad to 53 krad for this sector, indicating that when charge accumulation is performed intensively with Micron parts, the amount of charges in programmed cells as well as in disturbed cells can't be lowered enough by the irradiation to be read like "empty" cells.

However, the hardening effect is obtained thanks to charge accumulation for this reference when up to 100 write cycles are performed. But the benefit appears too late compared to the functionality loss, and the improvement represents less

than 1% of the data corruption. Within the limit of 1 000 write cycles, at the total dose level of 48 krad, the Micron memory behavior is similar to the Samsung devices at the beginning of their degradation. This assumption points out the device TID hardness importance when one wants to improve the data retention by multiple write cycles. As a consequence, this methodology would be more interesting for high dose applications.

IV. Heavy Ion Testing

After the TID tests, pristine NAND Flash memories of the same references were tested under heavy ion beam. The aim of this campaign was to study the impact on the SEU sensitivity of a similar approach with multiple write cycles. The heavy ion tests were conducted at the UCL (Université Catholique de Louvain – Belgium).

A. SEE test setup

The large capacity of the NAND Flash memories studied here is obtained by stacking several dies. A first campaign has been done to identify the top-most die, before starting the initialization phase. For this purpose, one sample of each reference has been delidded and filled with known data over the full memory depth. These two samples have been irradiated biased OFF, under Xe up to 10^7 cm^{-2}. The memory data post-analysis permitted the identification of the top-most dies.

The initialization process was done after selecting blocks and defining sectors in these dies. All parts were programmed with a checkerboard pattern. The numbers of pre-irradiation write cycles per sector as well as the sector sizes have been adapted for the heavy ion tests (Table III). After initialization, all sectors above 1 000 write cycles have shown disturbed cells in both references.

TABLE III
Write cycle sectors for SEU test

Part type	Sector number	Sector size (block [a])	Number of write cycles
Samsung	1	100	1
	2	100	10
	3	100	100
	4	50	1 000
	5	20	5 000
	6	20	10 000
	7	15	50 000
Micron	1	100	1
	2	100	10
	3	100	100
	4	50	1 000
	5	50	2 000
	6	10	5 000
	7	10	8 000

[a] Block size is 262 144 bytes for the Samsung parts, and 1 048 576 bytes for the Micron parts.

During the heavy ion test campaign, ten parts of each reference have been tested with 5 different LET values from 3.3 to 62.5 $MeV.cm^2.mg^{-1}$, with a flux of 5.10^3 $cm^{-2}.s^{-1}$ up to fluencies between 10^6 and 10^7 cm^{-2}.

All parts were unbiased under irradiation to avoid disturbance from possible critical event like SEL or SEFI. The data corruption measurement was performed at the end of each run, beam off, with the same test bench that was previously used for the TID tests. The measurement consists in reading the irradiated memory content sector by sector, and storing all corrupted data in separate files. When a part is irradiated several times, the data corruption evolution is obtained by comparison between the numbers of corrupted data before and after irradiation, so the recorded errors are cumulated. For example, a value of "zero" would indicate that the number of error is the same before and after irradiation.

The heavy ion species used during the SEE test campaign are given in Table IV.

TABLE IV
Ion species

Ion	Energy (MeV)	Range (µm(Si))	LET ($MeV.cm^2.mg^{-1}$)
$^{22}Ne^{7+}$	238	202	3.3
$^{40}Ar^{12+}$	379	120.5	10
$^{58}Ni^{18+}$	582	100.5	20.4
$^{84}Kr^{25+}$	769	94.2	32.4
$^{124}Xe^{35+}$	995	73.1	62.5

B. SEE test results

In this section, the heavy ion sensitivity in represented by the data corruption, computed as follow: the error number difference between after and before irradiation has been calculated, and expressed in ‰. This number as then been divided by the fluence. Moreover, the results presented here have been normalized with respect to the tested block number in order to be compared between each other and display the data corruption evolution. So the results presented here are neither data corruption percentages as presented in section III.B, nor common SEE cross-section – event number divided by the fluence.

Recovery effects have been observed for both part reference during the SEE test. When it was predominant, it led to negative values of the data corruption evolution. On Fig. 3, a linear scale is used to show this observation, in sectors where disturbed cells were initially present.

The following plotted values of data corruption are averaged over at least 2 cross section measurements on distinct devices for both references.

Samsung SEU test results

Fig. 3 shows the data corruption evolution for the Samsung memory. The number of write cycles has an impact on the data corruption: when the number of write cycle increases, the SEU sensitivity decreases. So in this case, the initialization is responsible for a hardening effect for the SEU cross section as well as for the TID tolerance.

Disturbed cells have only been created in sectors submitted to 1 000 preliminary write cycles and more. Sectors n° 2 and n°3 (10 and 100 write cycles) had no disturbed cells, and their initial content was free of error before irradiation. Therefore, no recovery effect could occur in these blocks and the improvement observed in Fig. 3 is then only attributed to the benefit of charge accumulation.

Fig. 3 also shows that for sectors widely corrupted by disturbed cells after initialization, the recovery effect is

predominant and the irradiation tends to reduce the global number of erroneous data. This recovery effect is more important at high LET.

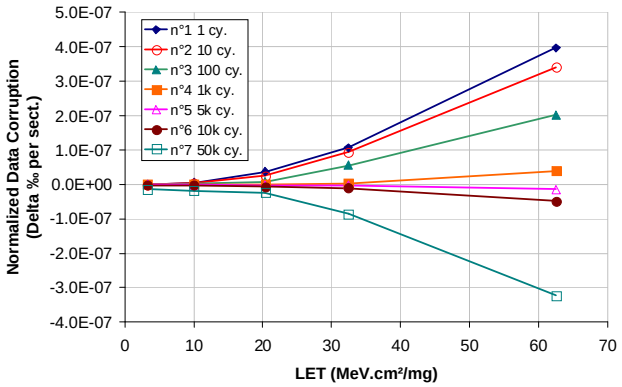

Fig. 3. Normalized Data Corruption versus LET – Samsung memory

Micron SEU test results

Fig. 4 shows that the SEU sensitivity has also been improved thanks to charge accumulation for the Micron parts.

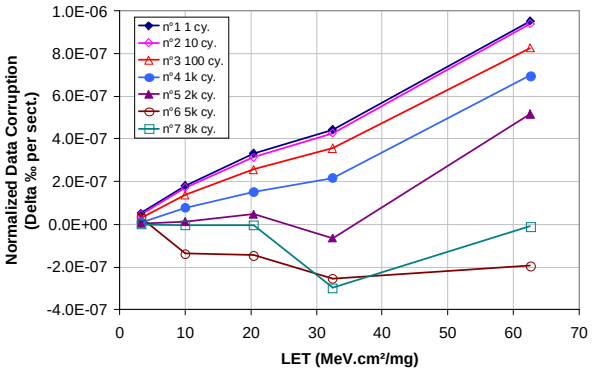

Fig. 4. Normalized Data Corruption versus LET – Micron memory

As previously observed during the TID test, the Micron parts have been sensitive to disturbed cells created by the initialization phase. Even by lowering the number of write cycles to a maximum of 8 000, the sectors n°6 and n°7 had almost 100% of their content corrupted after initialization. As a consequence, only negative values have been measured for these sectors. For sectors n°1 to n°5, Fig. 4 shows that the growing number of write cycles has a benefic impact on the data corruption evolution.

C. SEU post-analysis

NAND flash memories are known to be sensitive to SEU when submitted to heavy ions [1]. Within the framework of this study, the recovery effect on disturbed cells has also been observed. When reporting the total number of errors detected in a sector, one should consider that both phenomenon coexist and have an opposite trend on the device sensitivity.

In order to distinguish the SEU induced by heavy ions from corrected cells by recovery effect, the test data have been post-analyzed by comparing the test result files before and after irradiation. On the one hand, each address containing an error after irradiation that was not in the pre-irradiation file was considered as modified by ion-induced SEU. On the other hand, each address containing an error before irradiation that disappeared in the post-irradiation file was considered as modified by recovery effect (corrected cell). The particular case where the same address contains different data pre and post irradiation has also been treated. The principle of the post-treatment is illustrated on Fig. 5.

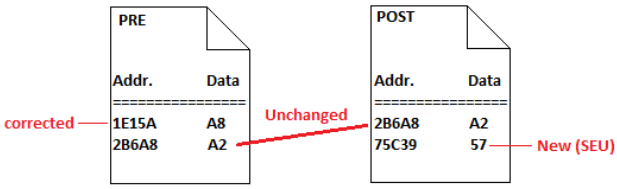

Fig. 5. SEE post-analysis principle

The post-treatment consists in calculating the difference between the post-irradiation error number and the pre-irradiation error number, taking into account the corrected cells. Once the SEU extracted from the results files, the cross section curves have been plotted.

Samsung SEU cross section

The SEU cross sections of the Samsung parts are presented on Fig. 6.

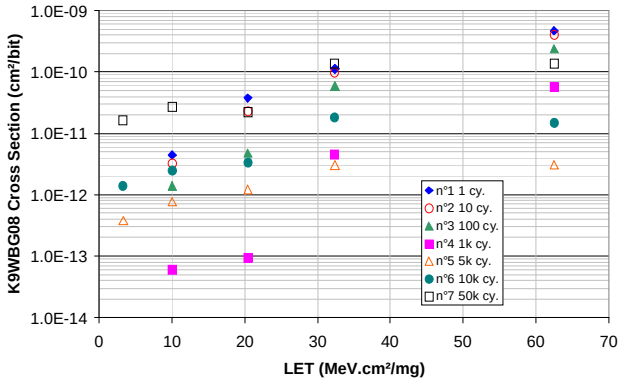

Fig. 6. Samsung memory SEU cross section

The memory radiation tolerance improvement is interesting when the number of write cycles is in the range of 10 to 1 000. Above 1 000 cycles, the behavior of the Samsung parts is degraded. For such sectors, events are observed at the lowest LET value of 3.3 MeV.cm².mg^{-1}, whereas it is not the case for sectors with a lower number of write cycles.

Micron SEU cross section

The Micron part SEU cross sections are presented on Fig. 7. Sectors n°6 and n°7, initialized with 5 000 and 8 000 write cycles, shows the worst behavior with an increased SEU sensitivity. With 1 000 write cycles, which represent the best case, the improvement is more important for low LET values.

Considering the results obtained for both the Micron and Samsung parts, the optimum has been observed around 1 000 preliminary cycles. The corresponding sectors always show an

interesting increase in the radiation tolerance, without significant degradation caused by the device initialization with multiple successive write cycles.

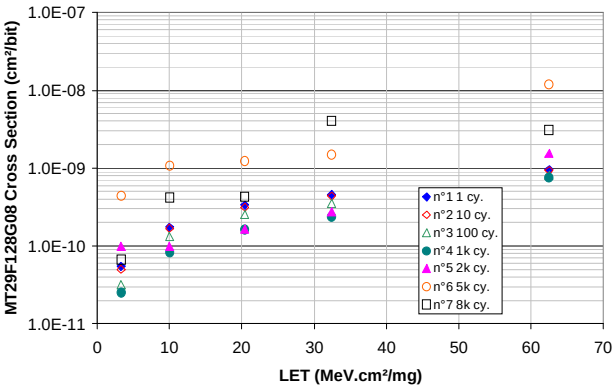

Fig. 7. Micron memory SEU cross section

V. Discussion

A. *Impact of multiple write cycles on the TID sensitivity*

Even if some small differences have been observed, both tested references are sensitive to charge accumulation. Concerning the Samsung parts, applying multiple write cycles improves the radiation tolerance by shifting up the dose level at which significant data corruption appears. With the memory standard use – storing data in a single write cycle – 50% of the data are corrupted at 125 krad, whereas it requires approximately 250 krad when 5 000 pre-irradiation write cycles are performed.

The Micron parts also show a slight improvement in data corruption when multiple write cycles are applied. However, the functionality loss occurs to early under TID exposure to allow a significant improvement.

For both Micron and Samsung parts, disturbed cells have been observed above 1 000 write cycles at the end of the initialization process. During the first irradiation steps, the amount of disturbed cells decreased (Fig. 1 and Fig. 2), whereas the reference parts – not irradiated – kept a constant number of errors. As a consequence, the recovery effect is attributed to radiations and not to the elapsed time. This effect is explained in [3]. Initial errors are due to parasitic charges that flow into adjacent cells during each write cycle as charges accumulate in the adjacent cells during write cycles, when the amount of charge is high enough, their content turn into a logic '0'. However, the charge level in these cells is lower than the accumulated charge in programmed cells. This is the reason why a correction effect is observed when the part is submitted to radiations. Radiation induced leakage currents remove charges from the disturbed cells, and when the latter fall under the detection limit, the expected data is read again, whereas the charge level is still high enough in programmed cells.

As a conclusion, the work presented here shows that there is a trade-off between the positive reduction of data corruption and the generation of disturbed cells, caused by the application of a large number of write cycles. This study shows that this trade-off is interesting in the order of 1 000 write cycles. In any case, one should stay far below the device endurance specification in order to avoid a too significant generation of disturbed cells. Finally, the test results also showed that the device TID hardness is important when one wants to improve the data corruption by multiple write cycles, because the sensitivity improvement started at several tenth of krad. As a consequence, this methodology would be interesting for high dose applications.

B. *Impact of multiple write cycles on the SEU cross section*

Concerning the SEU test results, the post-analysis results indicate that there is an optimum value for the number of write cycles. The best case is obtained when the number of write cycle is around 1 000 cycles – as for TID.

Above 1 000 write cycles, initial errors appear due to disturbed cells. The use of an alternate pattern (checkerboard) during SEE test has shown that the disturbed cell recovery effect could also be obtained with heavy ions.

Moreover, when too intensive write cycling is performed, a increase of the SEU sensitivity is observed. Concerning the Samsung parts, for 5 000 write cycles and more, the parts became more sensitive to SEU at the lowest LET value, and less sensitive at high LET values - the cross section curve was flattened. For the Micron parts, the SEU sensitivity is increased over the whole LET range beyond 2 000 cycles.

VI. Conclusion

The potentially hardening method based on charge accumulation developed in [3]-[5] has been applied on two commercial NAND Flash memories. An improvement of their radiation sensitivity has been observed for both TID and heavy ion test under certain conditions. An optimum, in terms of preliminary write cycle number, has been seen around 1 000 cycles for both tested references. Above this limit, two phenomenons have been observed: disturbed cells generation and SEU sensitivity increase.

The apparition of disturbed cells represents a significant limit to this method because it results in corrupted data, and the degradation of the SEU sensitivity is at the opposite of the expected effect. As a consequence, special cares should be considered before applying this method for hardening purposes.

Depending on the target application, applying a high number of write cycles may also have an impact on the system performance, due to the significant time required to store data when the number of cycle increases.

However, these issues appear when an excessive number of write cycles is applied, and the work presented here showed that a reasonable number of write cycles can lead to good results. Even at low cycle numbers, in the range of 10 to 100, a potentially hardening effect can be obtained.

This hardening method is also interesting because it can easily be applied in any design, just at software level. No additional hardware resource is required to improve the

radiation tolerance of NAND Flash memories, considering both TID and SEU sensitivity, but the write time increase can be significant. Finally, within the framework of this study, the impact of this method on the device reliability has not been covered and further investigation could be explored.

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